

V805-10

P682 DDR2

PCI-EXPRESSx16 DL-DVI VGA HDMI

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- 07/30
01. Create V805-0A base on MS-V804-0A change to DDR2 Memory
02. DDR2 Memory schematic copy from MS-V202-0A
03. Reserve GPIO[5:6] NVVDD switch · NVVDD state = 0.9V(00) · 1V(10) · 1.0625V(11)
04. remove JTAG
05. remove HDCP ROM
06. remove FAN control · for 12V full speed
07. remove DAC EMI filter & ESD Diode & remove pi type left side cap
08. modify 5V circuit to TO-252 package
09. remove PWM NVVDD OCSET · Chage 10Kohm parallel low-side MOSFET VGS
10. remove R576 net IFP_PLLVDD change to 3V3
11. decrease caps
12. modify NVVDD & FBVDD PWM compensation value
13. MIOA_VDDQ net to GND · MIOA_CLKIN net to NC
14. del PEX_PLLVDD SUPPLY circuit
15. add NVVDD & FBVDD 12V input SMD choke overlap 0805 / 0 ohm
16. NVVDD & FBVDD 12V input DIP cap change to 3 pin
17. overlap NVVDD & FBVDD output choke

- 05/07
- Page 01 1.Remove C690,C70 47uF
- Page 10 1.Remove J1 D-Sub
- Page 11 1.Remove R16,Q2
- Page 12 1.Remove R1,Q1
- Page 16 1.Change Crystal Footprint to 2-PIN SMD
- 2.Remove C71 47uF
- 05/08
- Page 17 1.Remove Thermal Sensor Circuit
- Page 18 1.Remove U2,C54,R31,R30,D16 INFOROM circuit
- Page 19 1.Remove 3V3 to 1.8V circuit
- 2.Change 5V REGULATOR Circuit
- Page 20 1.Change L8 Footprint to 1.6uH
- 2.Change Footprint to multi cap for EL 1500uF
- Page 21 1.Change NVVDD to UP6161
- 2.Change L12 footprint to 1.2uH
- 05/10
- Page 05 1. Remove Decoupling for EMI cap
- Page 20 1. C84 change Footprint to multi cap
- 05/11
- Page 21 1.Add C39 270uF
- 2.Add R922,R924 for APW7068 OCSET
- Page 16 1.Add XTALIN R566 Resister
- Add XTALOUT R573 Resister
- Page 02 1.Change C51 to 0805 1UF and ADD C54 0805 1UF
- Page 03 1.C642,C666,C633 change to .01UF
- Page 05 1.Remove C516,C525,C549,C556,C541,C512
- Remove C513,C546,C540,C528,C547,C507
- Remove C544,C545,C520,C523,C532,C508
- Remove C535,C526,C543,C553,C537,C88
- Page 08 1.Remove C566,C567,C576,C578,C82,C564
- Remove C619,C592,C586,C585,C622,C574
- Remove C705,C706,C680,C729,C691,C683
- Remove C742,C738,C731,C725,C743,C728
- Page 20 1.Remove C86,C562,C563,C87

- 05/12
- Page 17 1.Remove 4-PIN FAN Circuit
- Page 12 1.Change Q509 to Q513,Q514 SOT23 footprint
- Page 16 1.Change FAN Screw hole
- Page 20 1.Add C102 820uF
- 05/14
- Page 21 1.Remove D94 scottky diode
- 05/19
- Page 11 1.Add EMI bridge
- Page 12 2.Add EMI bridge
- 05/21
- Page 03 1.Add RP24 termination risister
- Page 06 2.Add RP23 termination risister
- 05/26
- SWAP CMD
- Page 03/06 RP5.1 · RP5.2 FBC_CMD10 · RP5.3 · RP5.4 FBC_CMD22
- RP4.1 · RP4.2 FBC_CMD18 · RP4.3 · RP4.4 FBC_CMD7
- RP24.1, RP24.2 FBA_CMD30, RP24.3, RP24.4 FBA_CMD7
- RP20.1, RP20.2 FBA_CMD14, RP20.3, RP20.4 FBA_CMD18
- RP14.1, RP14.2 FBA_CMD1, RP14.3, RP14.4 FBA_CMD20
- RP12.3, RP12.4 FBA_CMD29
- 05/27
- Page 05 1. Add Decoupling for EMI cap C80,C524,C517,C102

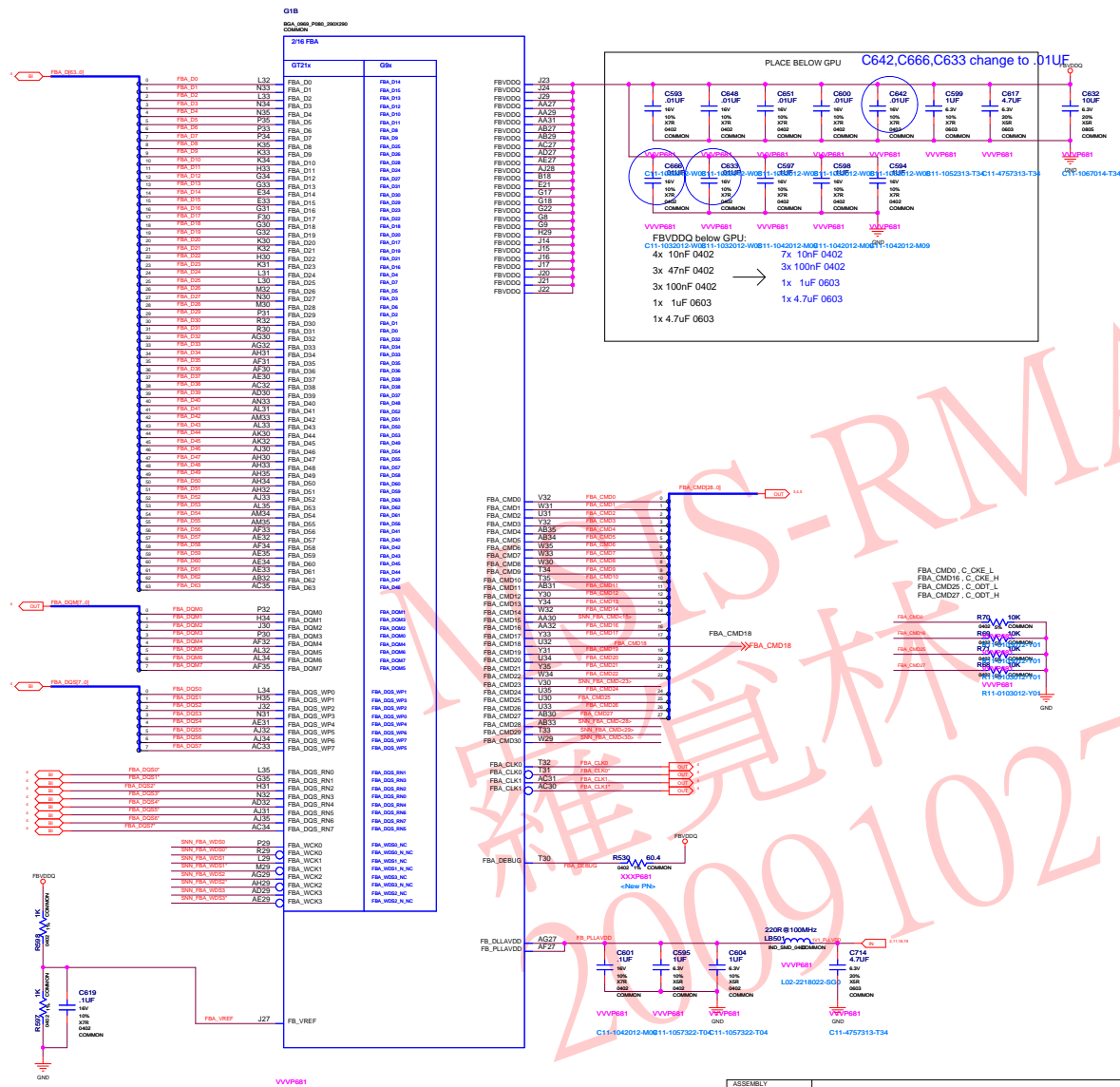
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B	BASE	600-10681-0000-100	BASE LEVEL GENERIC SCHEMATIC ONLY COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU001	600-10681-0001-100	GT215-300 6001500MHz 1024MB 64Mx16 BGA100 900MHz DDR3 DVI-VGA+HDMI
2	SKU002	600-10681-0002-100	GT215-300 6001500MHz 1024MB 64Mx16 BGA100 1000MHz DDR3 DVI-VGA+HDMI
3	SKU0011	600P0681-0011-100	GT215-300 6001500MHz 1024MB 64Mx16 BGA100 900MHz DDR3 DVI-VGA+HDMI
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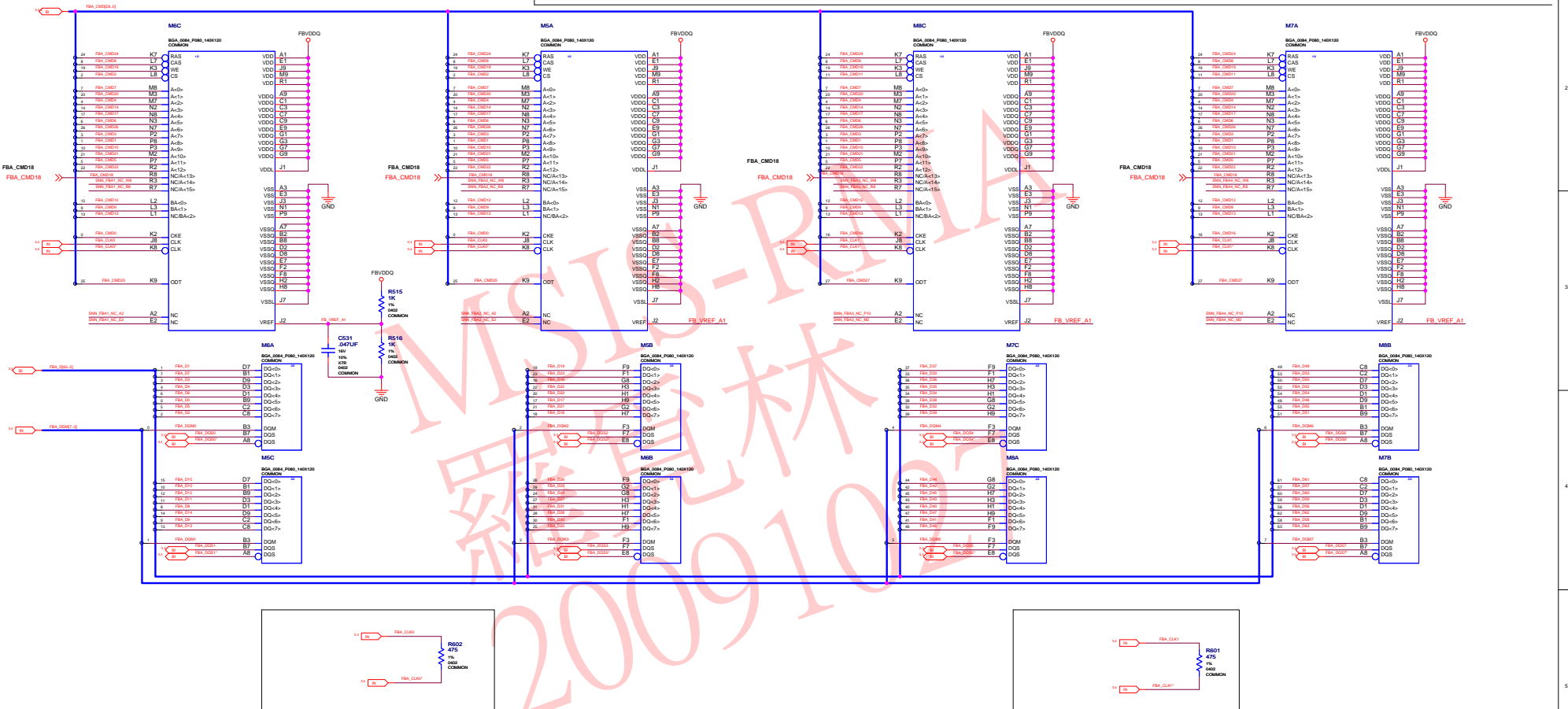


PARTITION A FRAME BUFFER INTERFACE



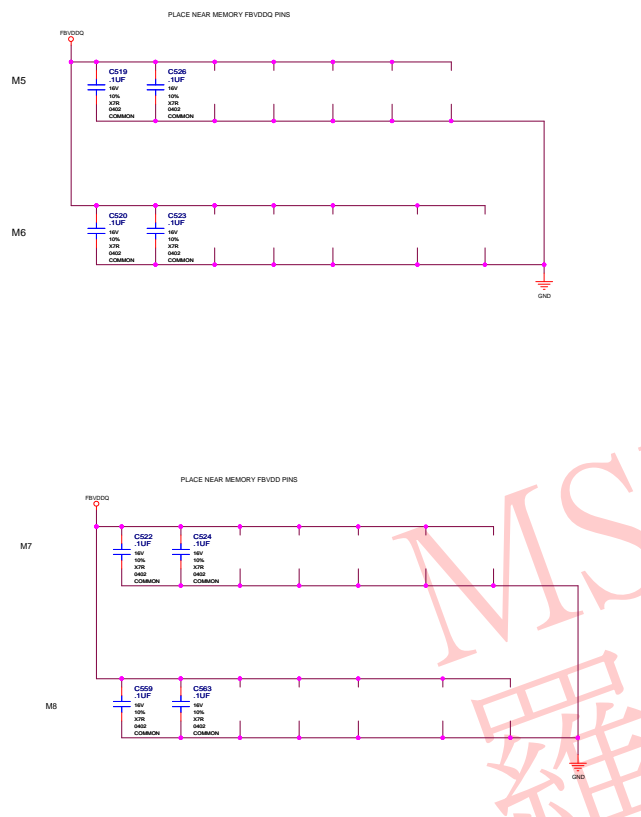
Partition A Memories

GT21x CMD MAP

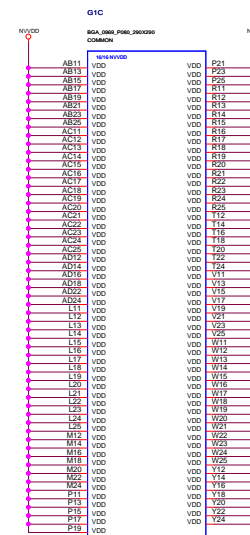
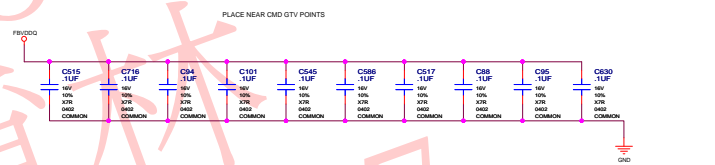


FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS

Decoupling for FBA



Return path coupling GND/FBVDDQ



VVVP681

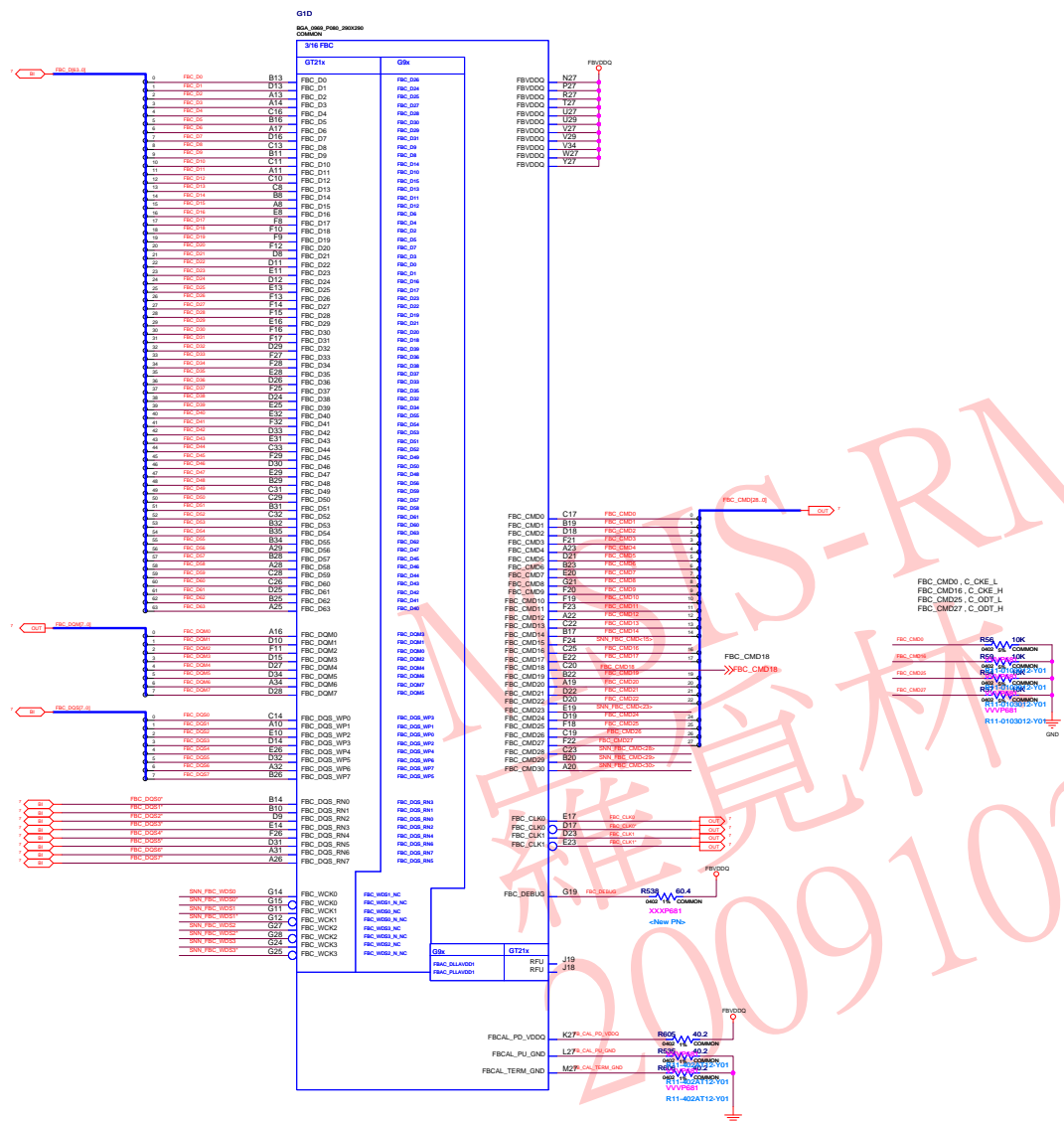
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FBA DECOUPLING CAPS & NVVDD DECOUPLING CAPS

PARTITION C FRAME BUFFER INTERFACE



VVVP681

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PARTITION C FRAME BUFFER INTERFACE

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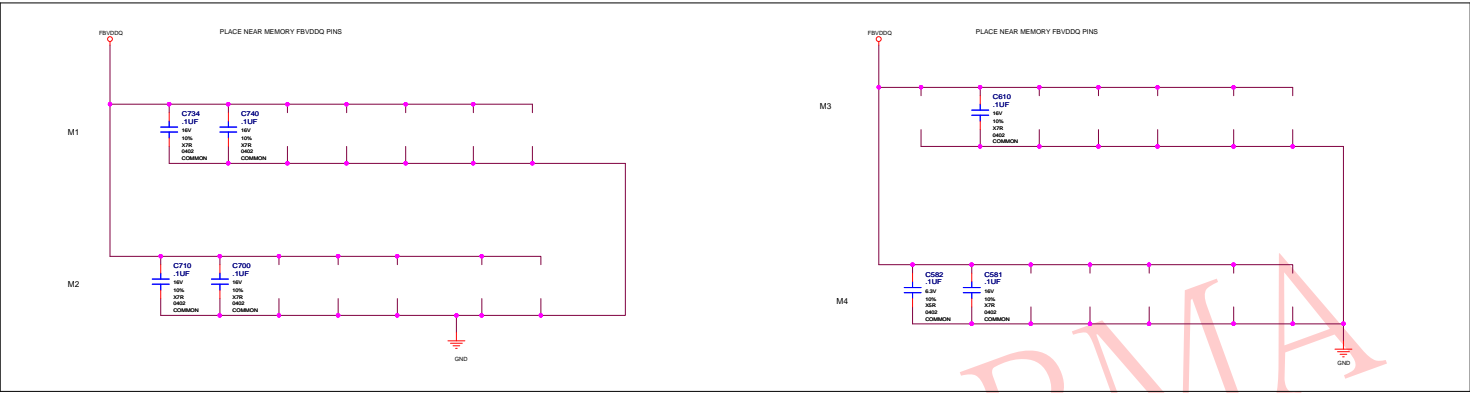


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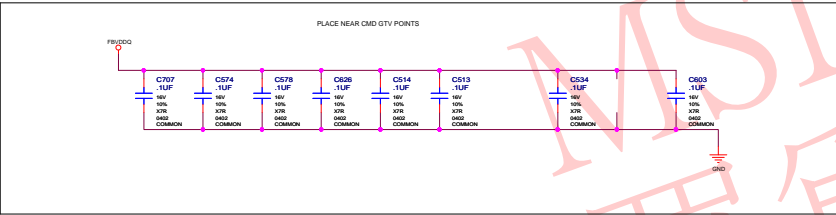
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FBC DECOUPLING CAPS & NVVDD DECOUPLING CAPS

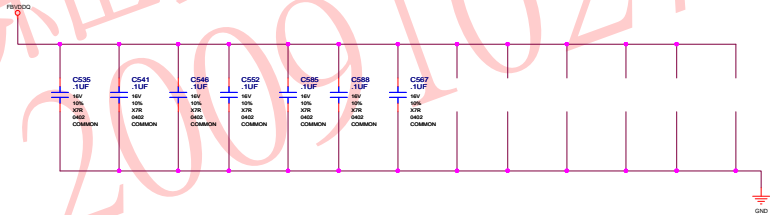
Decoupling for FBC



Return path coupling GND/FBVDDQ



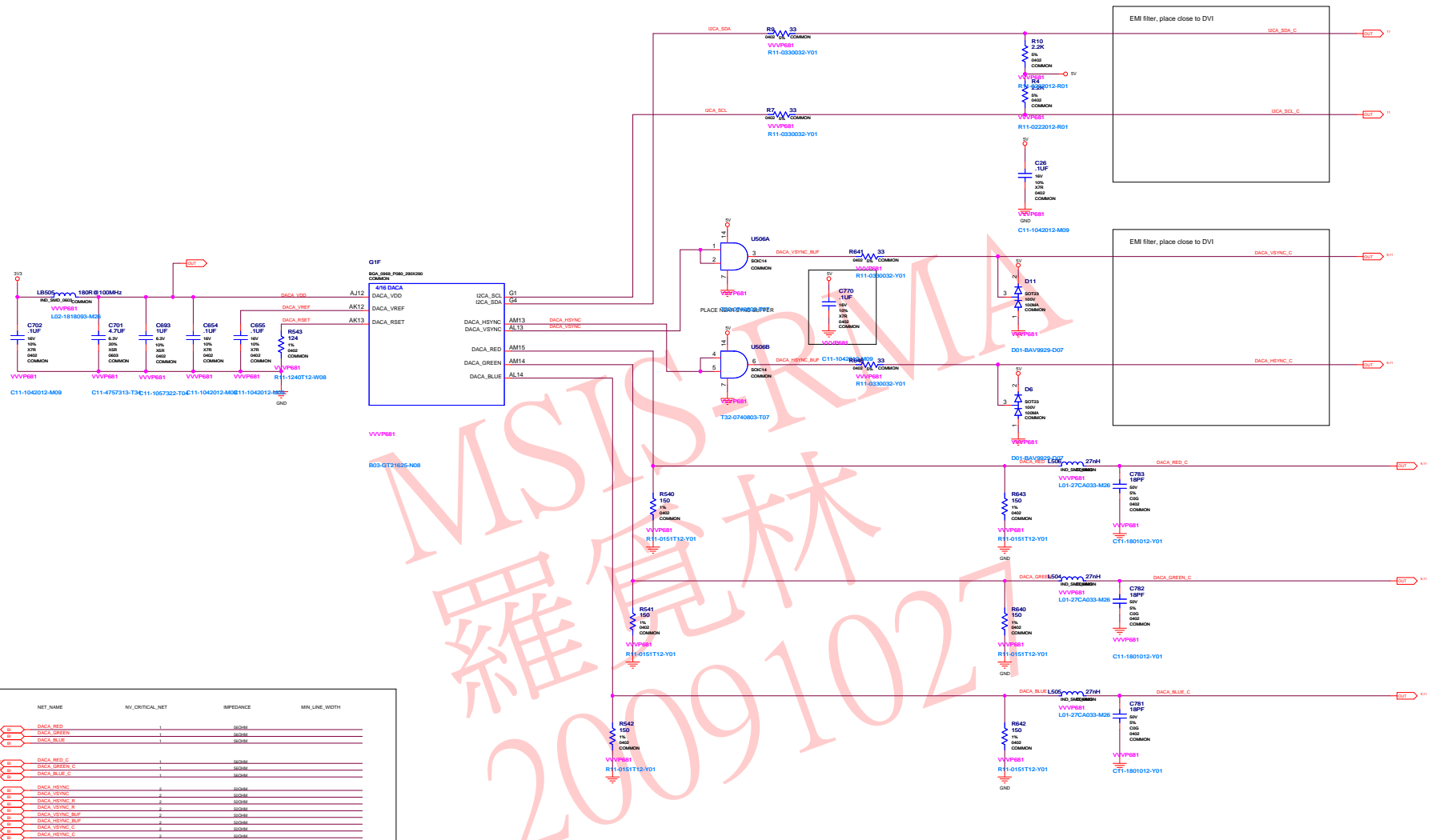
Return path coupling GND/FBVDDQ for FBA/FBC



Pin list table showing connections for various pins (AA11 to Y25) to GND or VVVPB1.

AA11	GND	E15	GND
AA12	GND	E18	GND
AA13	GND	E24	GND
AA14	GND	E27	GND
AA15	GND	E30	GND
AA16	GND	E6	GND
AA17	GND	E8	GND
AA18	GND	E9	GND
AA19	GND	F31	GND
AA20	GND	F34	GND
AA21	GND	F5	GND
AA22	GND	F6	GND
AA23	GND	F31	GND
AA24	GND	F34	GND
AA25	GND	J5	GND
AA26	GND	L3	GND
AA27	GND	M11	GND
AA28	GND	M15	GND
AA29	GND	M19	GND
AA30	GND	M2	GND
AA31	GND	M21	GND
AA32	GND	M22	GND
AA33	GND	M25	GND
AA34	GND	M26	GND
AA35	GND	M31	GND
AA36	GND	M34	GND
AA37	GND	M6	GND
AA38	GND	M11	GND
AA39	GND	M12	GND
AA40	GND	M13	GND
AA41	GND	M14	GND
AA42	GND	M15	GND
AA43	GND	M16	GND
AA44	GND	M17	GND
AA45	GND	M18	GND
AA46	GND	M19	GND
AA47	GND	M20	GND
AA48	GND	M21	GND
AA49	GND	M22	GND
AA50	GND	M23	GND
AA51	GND	M24	GND
AA52	GND	M25	GND
AA53	GND	M26	GND
AA54	GND	M27	GND
AA55	GND	M28	GND
AA56	GND	M29	GND
AA57	GND	M30	GND
AA58	GND	M31	GND
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AA66	GND	M39	GND
AA67	GND	M40	GND
AA68	GND	M41	GND
AA69	GND	M42	GND
AA70	GND	M43	GND
AA71	GND	M44	GND
AA72	GND	M45	GND
AA73	GND	M46	GND
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AA75	GND	M48	GND
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AA367	GND	M340	GND
AA368	GND	M341	GND
AA369	GND	M342	GND
AA370	GND	M343	GND
AA371	GND	M344	GND
AA372	GND	M345	GND
AA373	GND	M346	GND
AA374	GND	M347	G

DACA (SOUTH DVI-I)



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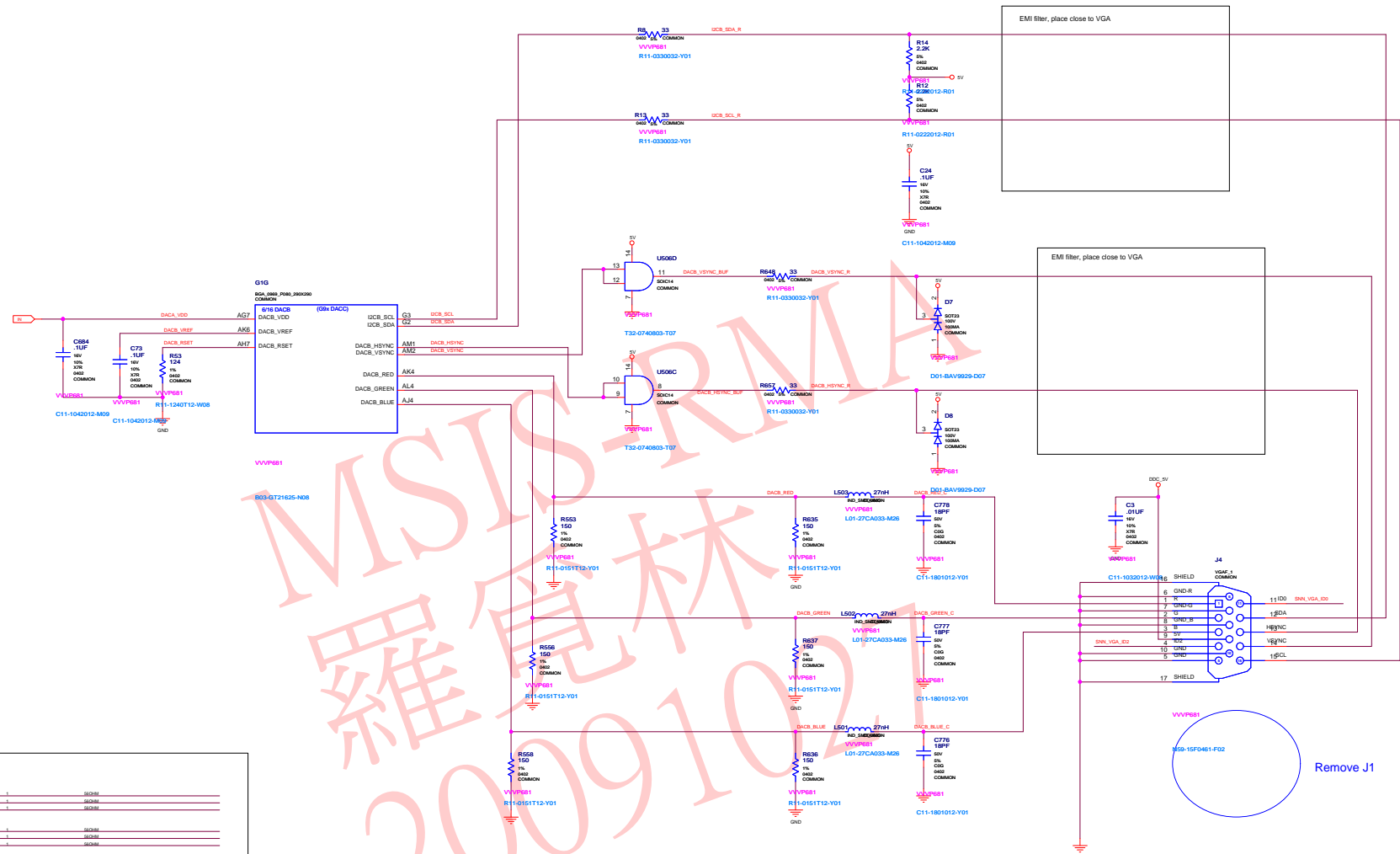
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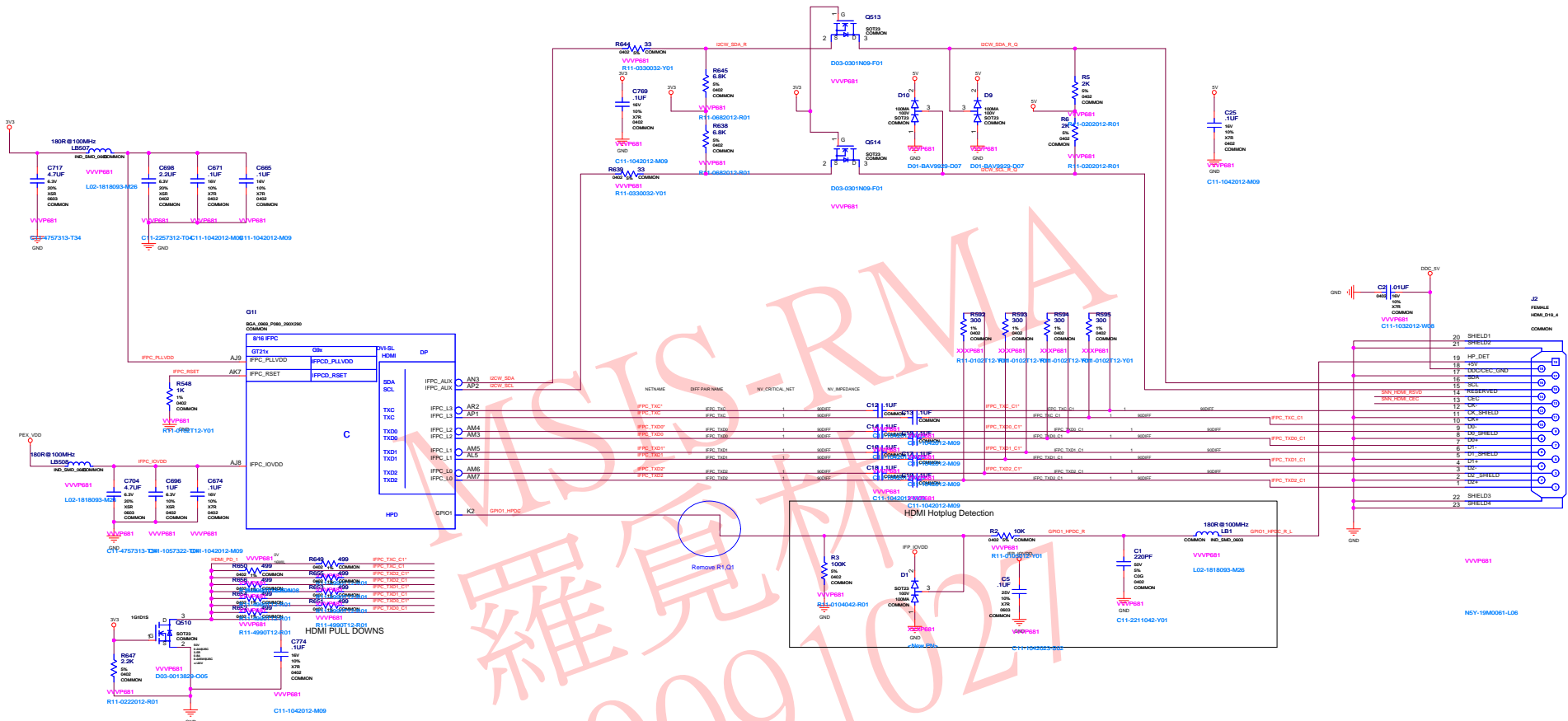
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DACB (MID VGA)



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IFP C (NORTH HDMI)

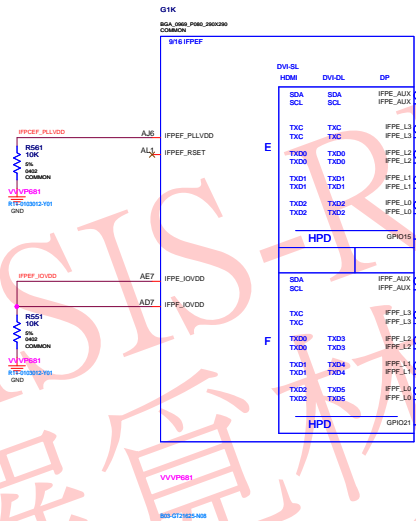


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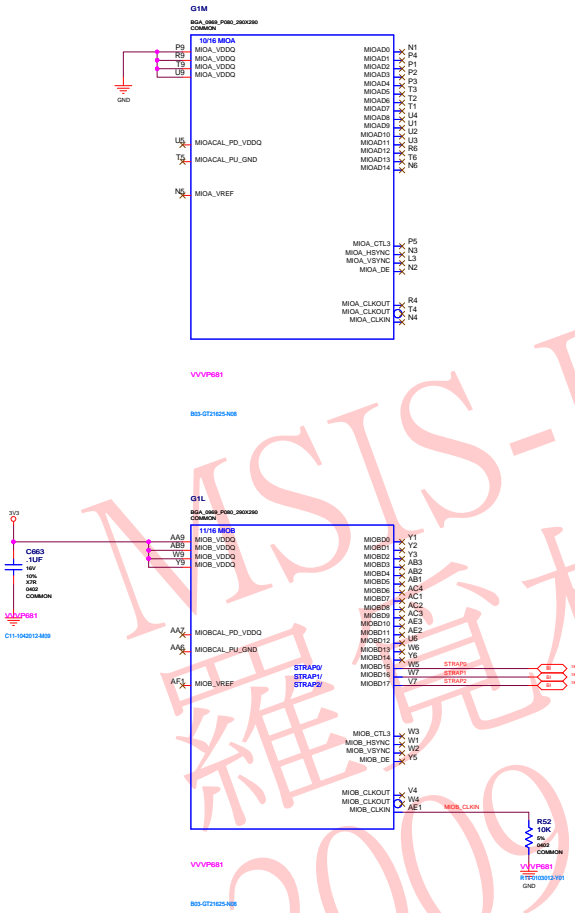


IFP EF (UNUSED)



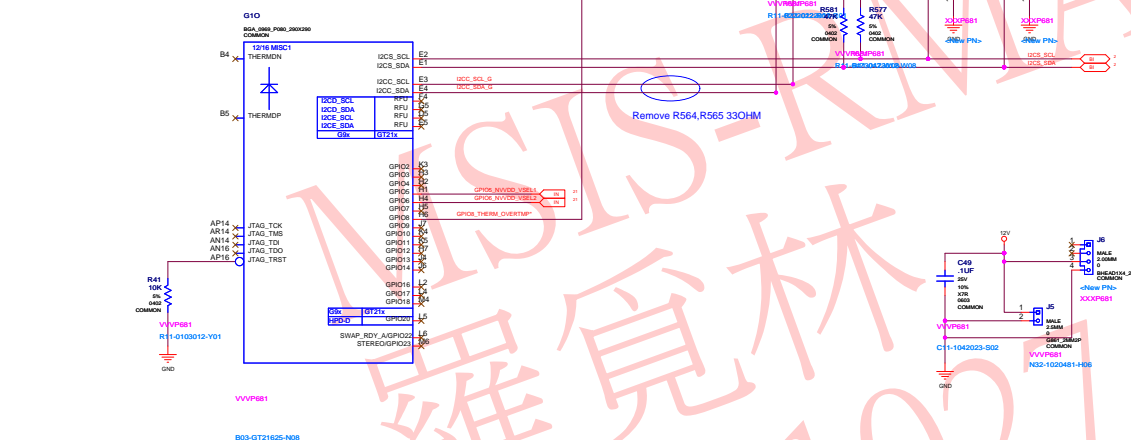
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MIOA & MIOB



THERMAL SENSOR

~~I2C: 0x4CH~~



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	EXTERNAL THERMAL SENSOR, FAN CONTROL, GPIO, JTAG

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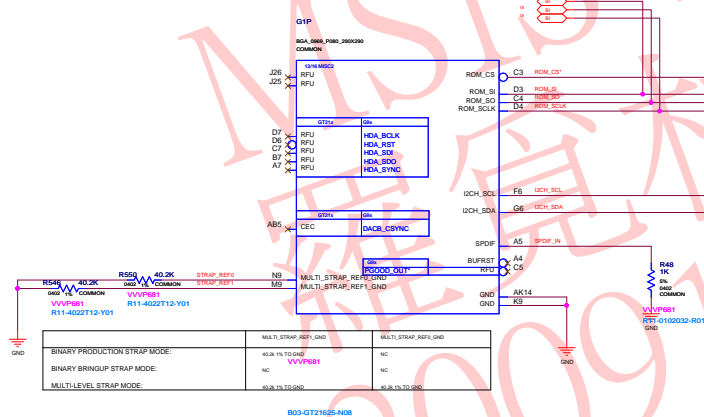
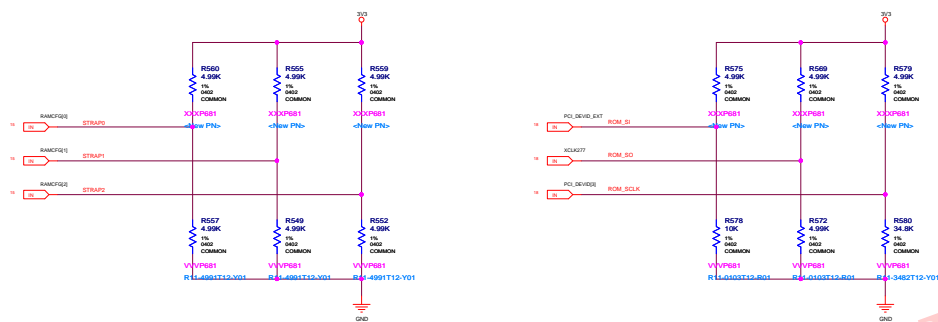


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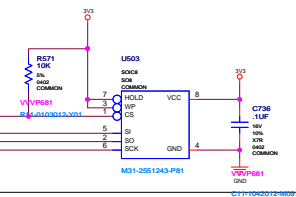
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BIOS ROM, HDCP ROM, STRAPPING OPTIONS

STRAPPING OPTIONS

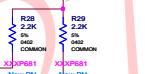


BIOS ROM(serial)



For Lab Use Only

HDCP I2C EEROM



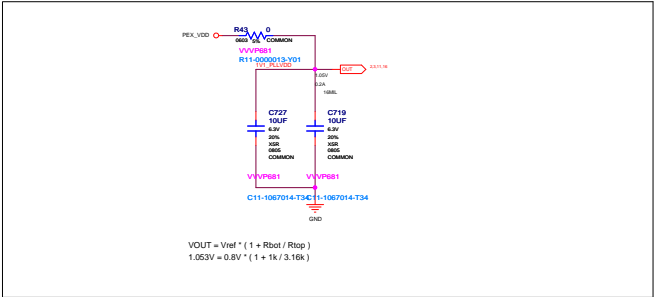
INFOROM

For Lab Use Only
INC ADDRESS

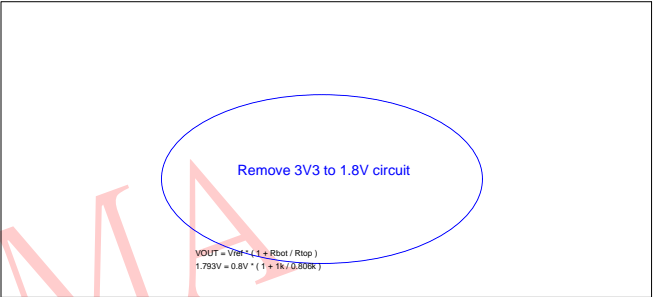
Remove
U2,C54,R31,R30,D16
INFOROM

LINEAR POWER SUPPLIES

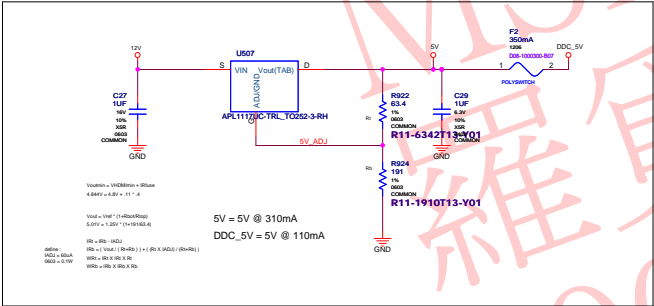
PEX_PLLVDD SUPPLY (OPTIAN)



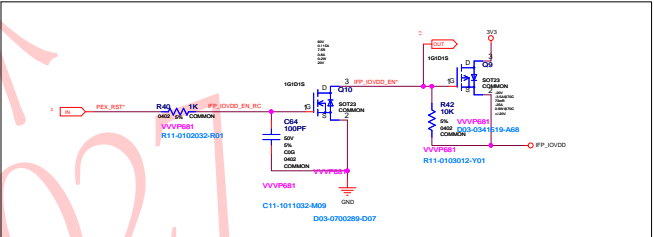
IFP_PLLVDD SUPPLY



5V & DDC_5V REGULATOR



IFP_IOVDD BACKDRIVE PREVENTION



FBVDDQ/PEXVDD POWER SUPPLY

PEXVDD = 1.05V @ 3A

$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$
 $1.05V = 0.8V * (1 + 1.00k / 3.16k)$

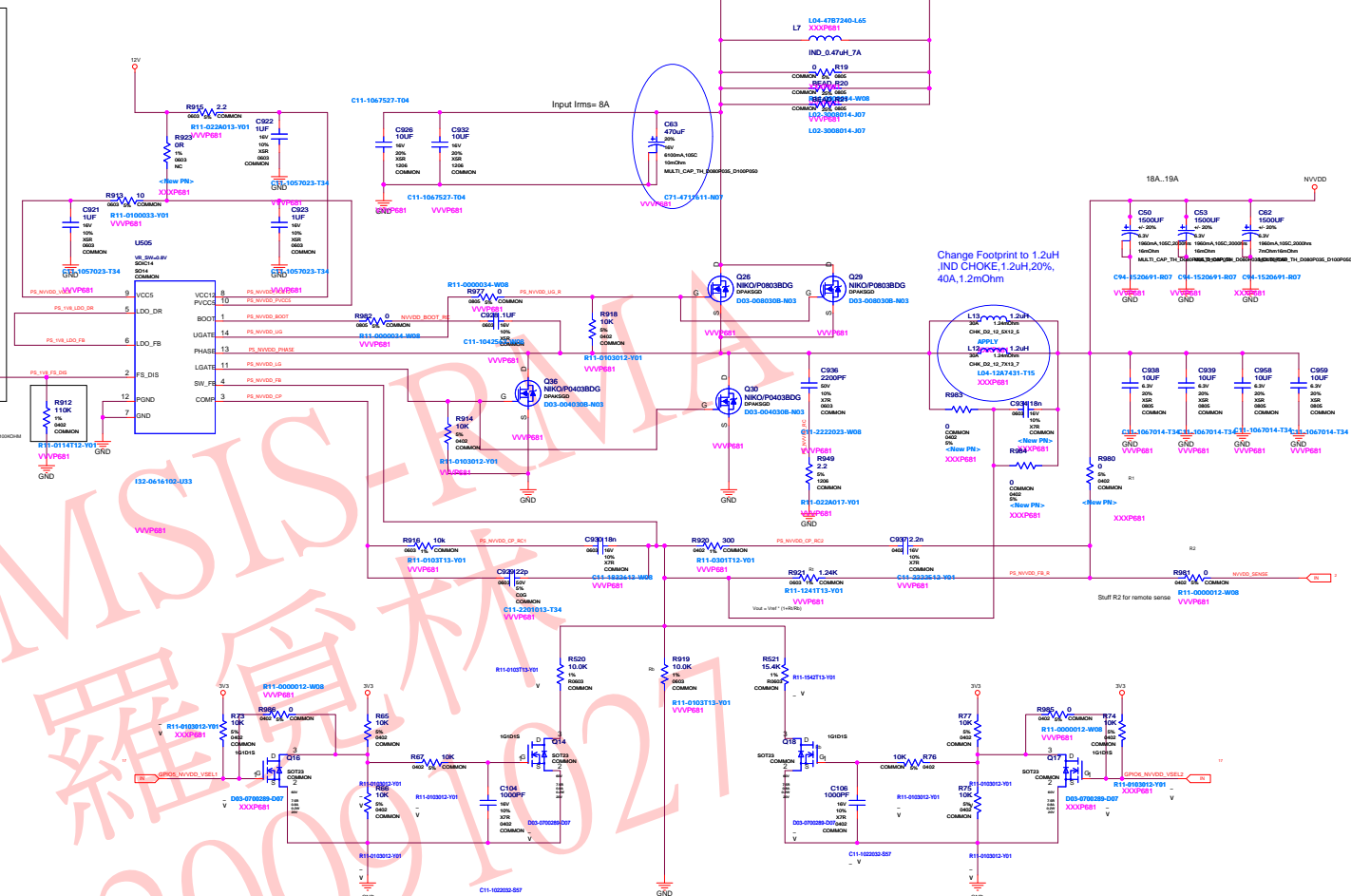
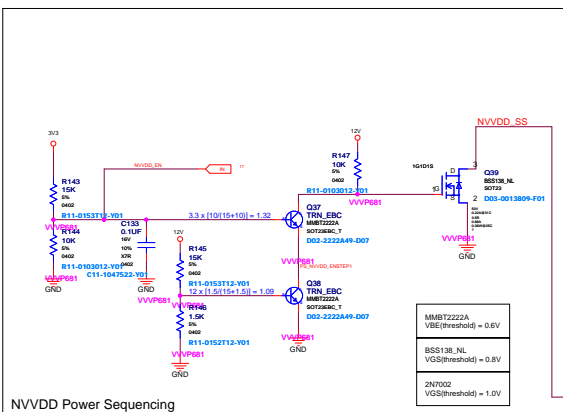
$FBVDDQ = V_{ref} * (1 + R_{top} / R_{bot})$
 $1.50V = 0.8V * (1 + 1.58k / 1.82k) @ GPIO13 = 0$
 $1.8V = 0.8V * (1 + 1.58k / 1.27k) @ GPIO13 = 1 (DEFAULT)$

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PROCESS DETAIL	78VDDQ/PEXVDD POWER SUPPLY

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Power Supply III: NVVDD



$V_{out} = V_{ref} * (1 + R_t/R_b)$
 $V_{out} = 0.8 * (1 + 1.24k/R_{bn})$
 $R_{b1} = R919$
 $R_{b2} = R919 // R520$
 $R_{b3} = R919 // R520 // R521$

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